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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,589	08/28/2001	Keiki Watanabe	ASA-1026	3261

7590 06/02/2004

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,589	WATANABE ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/28/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is missing.

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the Application Number and Filing Date, is required.

Drawings

2. The drawings are objected to because

- In figure 1, the direction of the arrow for "Transmission side input data" is incorrect. The direction of the arrow for "Transmission side input data" should be towards "Transmitting Circuit".
- In figure 2, the direction of the arrows for "Reception side input data" is incorrect. The direction of the arrow for "Reception side input data" should be towards "Receiving Circuit".
- In figure 2, the direction of the arrows for "Reception side output data" is incorrect. The direction of the arrows for the "Reception side output data" should be towards "Operation judging apparatus".

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Figure 4, 5 and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al. (US 5,787,114) in view of Sasaki et al. (US 4,833,395) and Funatsu (US 4,225,958).

As per claim 1, Ramamurthy et al. teach a semiconductor integrated circuit formed on a single semiconductor chip (col. 4, lines 43-45, Ramamurthy et al.), comprising: a test mode input terminal supplied with a test mode signal (figure 3, col. 7, lines 17-19, Ramamurthy et al.); a transmitting circuit having a function of converting first parallel signals for a plurality of channels to a first serial signal (figure 3, col. 6, lines 66-67, col. 7, lines 1-7, Ramamurthy et al.); a receiving circuit having a function of converting a second serial signal to second parallel signals for a plurality of channels (deserializer 12 in figure 3, col. 7, lines 7-10, col. 8, lines 50-51, Ramamurthy et al.); a test signal generating circuit responsive to said test mode signal, for generating test parallel signals to be supplied to said transmitting circuit, wherein said test signal generating circuit comprises a first circuit for generating test parallel signals that are equivalent to said first parallel signals for a plurality of channels (figure 3, col. 7, lines 20-22, Ramamurthy et al.); a second selector responsive to said test mode signal, for supplying either said first serial signal supplied from said transmitting circuit or said second serial signal to said receiving circuit (switching circuit 25 in figure 3, col. 7, lines 35-40, col. 8, lines 36-44, Ramamurthy et al.);

and an operation judging circuit responsive to said test mode signal, said operation judging circuit being connected so as to receive response parallel signals from said receiving circuit, wherein said operation judging circuit comprises: a plurality of third circuits for generating expected values for pulses of pulse sequences in the response parallel signals received from said receiving circuit after the pulses whose signal values have been held, based on signal values held in said second circuits; and a plurality of fourth circuits for comparing values of pulses of the pulse sequences in the response parallel signals

received from said receiving circuit with the expected values generated by said third circuits (figure 3, col. 7, lines 52-58, Ramamurthy et al.).

However Ramamurthy et al. do not explicitly teach the specific use of a first selector for supplying either said test parallel signals generated by said test signal generating circuit or said first parallel signals to said transmitting circuit and each of said test parallel signals includes a pulse sequence, and each of said response parallel signals includes a pulse sequence.

Sasaki et al. in an analogous art teach that during the normal operation of the LSI when no test is carried out, the output signal of the input buffer 13 is switched from the test signal to the external input signal from the external input terminal 28 by applying the low-level signal to the test external terminal 21, and the logic circuit 14 is operated by the external input signal (col. 4, lines 58-64, Sasaki et al.). Sasaki et al. also teach that a pulse signal Vp3 shown in FIG. 6c is obtained from the NAND circuit 26 as the test signal (figure 3, 6, col. 6, lines 3-4, Sasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ramamurthy et al.'s patent with the teachings of Sasaki et al. by including an additional step of using a first selector for supplying either said test parallel signals generated by said test signal generating circuit or said first parallel signals to said transmitting circuit and each of said test parallel signals includes a pulse sequence, and each of said response parallel signals includes a pulse sequence. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to test the integrated circuit using the test signal generating circuit when needed or the integrated circuit can be used as a data transmitter / receiver in a normal operation. Using test parallel signals including pulse sequence would provide the opportunity to change the frequency of the pulse sequence for the test signal as desired depending on the transmitting / receiving circuit test.

Ramamurthy et al. also do not explicitly teach the specific use of a plurality of second circuits each capable of holding a value of one pulse in its associated one of the pulse sequences of said response parallel signals received from said receiving circuit.

However Funatsu in an analogous art teaches that in the test mode, the second holding circuits 37 select the electronic circuit output signals or the second data output signals and hold the selected signals. Turning to FIG. 3, an elementary circuit 40 used as each of the first and the second holding circuits 36 and 37 preferably comprises first and second circuits 41 and 42. The latch circuit 65 holds the first selected signal S1 (figure 3, col. 5, lines 21-24, lines 27-30, col. 6, lines 58-59, Funatsu).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ramamurthy et al.'s patent with the teachings of Funatsu by including an additional step of using a plurality of second circuits each capable of holding a value of one pulse in its associated one of the pulse sequences of said response parallel signals received from said receiving circuit.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to compare the received signal with the expected signal and determine the bit error rate and analyze the error information.

- As per claim 2, Ramamurthy et al., Sasaki et al. and Funatsu teach the additional limitations. Sasaki et al. teach a semiconductor integrated circuit wherein when the test parallel signals constitute such a multi-bit signal that each pulse of a pulse sequence in each of the test parallel signals forms one bit (figure 6, col. 6, lines 3-4, Sasaki et al.), the first circuit comprises: a plurality of first flip-flop circuits for sending out said multi-bit test parallel signals; a plurality of second flip-flop circuits disposed in a stage preceding that of said first flip-flop circuits; and a plurality of exclusive OR circuits each for comparing values of two bits located at a distance of a predetermined number of bits between and included in bits of the test parallel signals supplied from said plurality of first flip-flop circuits, and supplying a result of the comparison to corresponding one of said plurality of first flip-flop circuits (figure 7, col. 6, lines 36-63, Sasaki et al.).

7. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al. (US 5,787,114), Sasaki et al. (US 4,833,395) and Funatsu (US 4,225,958) as applied to claim 2 above, and further in view of Ushikoshi (US 4,545,686).

As per claim 3, Ramamurthy et al., Sasaki et al. and Funatsu substantially teach the claimed invention described in claim 2 (as rejected above).

However Ramamurthy et al., Sasaki et al. and Funatsu do not explicitly teach the specific use of a semiconductor integrated circuit, wherein said operation judging circuit comprises an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits.

Ushikoshi in an analogous art teaches that the circuit of FIG. 7 comprises exclusive NOR gates 129-136 and AND gates 128, 137 for the coincidence circuits 113, 115 (figure 7, col. 9, lines 36-39, Ushikoshi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ramamurthy et al.'s patent with the teachings of Ushikoshi by including an additional step of using a semiconductor integrated circuit, wherein said operation judging circuit comprises an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to use the logic circuits to implement the comparison circuit to determine errors in the integrated circuit.

- As per claim 4, Ramamurthy et al., Sasaki et al., Funatsu and Ushikoshi teach the additional limitations.

Ushikoshi teaches an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits; a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal; and an SR latch circuit that is set by an output of said third flip-flop circuit (figure 7, col. 9, lines 36-39, col. 10, lines 8-21, Ushikoshi).

- As per claim 5, Ramamurthy et al., Sasaki et al., Funatsu and Ushikoshi teach the additional limitations.

Ushikoshi teaches the operation judging circuit comprises: an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits (figure 7, col. 9, lines 36-39, Ushikoshi); a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal; an SR latch circuit that is set by an output of said third flip-flop circuit (figure 7, col. 10, lines 8-21,

Ushikoshi); and a reset circuit for canceling a reset state of said SR latch circuit upon elapse of a predetermined time after a circuit disposed in a stage preceding that of said SR latch circuit is reset (figure 1, col. 5, lines 5-8, Ushikoshi).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al. (US 5,787,114), Sasaki et al. (US 4,833,395) and Funatsu (US 4,225,958) as applied to claim 1 above, and further in view of Katayama (US 5,353,434).

As per claim 6, Ramamurthy et al., Sasaki et al. and Funatsu substantially teach the claimed invention described in claim 1 (as rejected above). Ramamurthy et al. teach the test signal generating circuit (figure 3, col. 7, lines 20-22, Ramamurthy et al.) and the operation judging circuit (figure 3, col. 7, lines 52-58, Ramamurthy et al.).

However Ramamurthy et al., Sasaki et al. and Funatsu do not explicitly teach the specific use of a clock having a frequency corresponding to a transfer rate of said first or second parallel signals.

Katayama in an analogous art teaches generating a first clock Signal at a frequency corresponding to a predetermined data transfer rate between the recording medium and the reader/writer (col. 13, lines 28-32, Katayama).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ramamurthy et al.'s patent with the teachings of Katayama by including an additional step of using a clock having a frequency corresponding to a transfer rate of said first or second parallel signals.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to align and synchronize the parallel test data transmitted and received for comparison to determine bit error rate of the circuits.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

Albert DeCady
Primary Examiner